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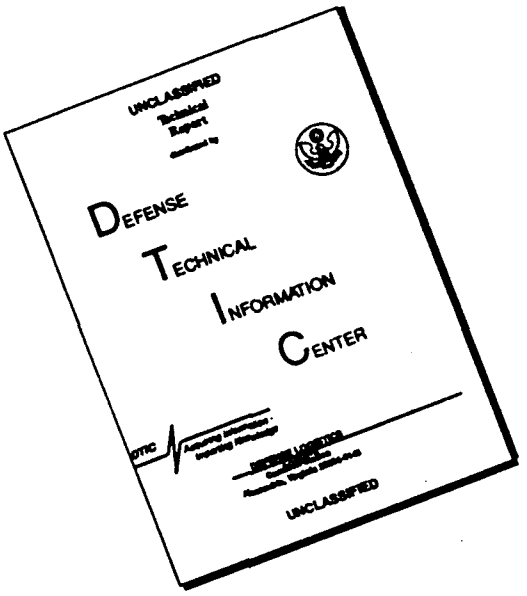

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SUPERCONCURRENCY

A Form of Distributed Heterogeneous Supercomputing

BY RICHARD F. FREUND AND D. SUNNY CONWELL
NAVAL OCEAN SYSTEMS CENTER (NOSC)

Introduction

Some of the complex issues of future supercomputing are discussed in the Richard Hill and John Gustafson papers published in the June 1990 issue of *Supercomputing Review*. Both papers contemplate the role of parallel processors in future operational environments. We explore here a variation of Gustafson's suggested approach, heterogeneous parallelism, focusing in particular upon Distributed Heterogeneous Supercomputing (DHS). DHS is the use of a heterogeneous suite of diverse processors — e.g., a mix of vector and parallel computers.

DHS is not simply a LAN or a WAN because it aims to exploit the heterogeneous nature of the suite for reasons such as access to different data bases, access to remote special processors, or super-speed performance.

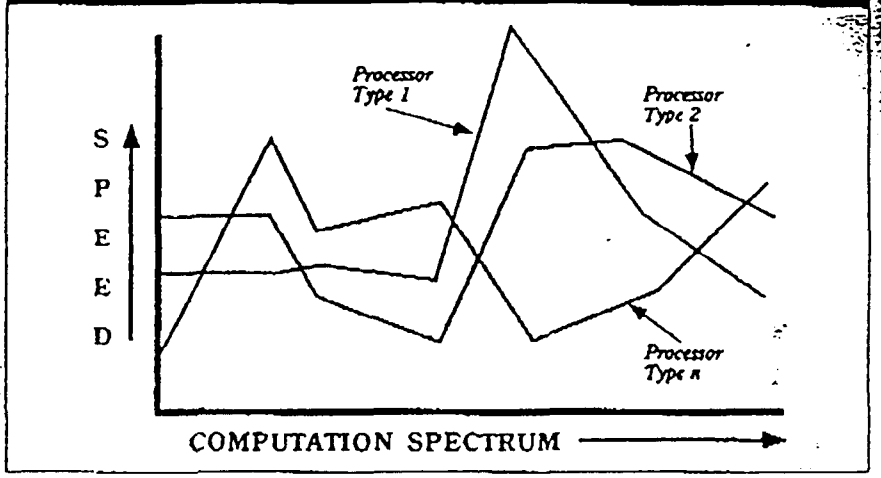
Performance is the key to the Superconcurrency (Super-C) form of DHS, because Super-C tunes the selection of the different processors and distributes the work optimally, primarily for maximum performance on the problem at hand and only secondarily for load balancing.

Types of Concurrency

There are a number of variant factors that enter into classifications of concurrent ("multiplicity") processing, e.g., memory organization (distributed, global, hierarchical, etc.) or processor interconnect scheme (bus, mesh, hypercube, etc.). Perhaps the most basic distinction is whether the processors execute the fine-grain parallelism of same instruction on multiple data (SIMD or vector) or the procedural parallelism of multiple instructions on multiple data (MIMD).

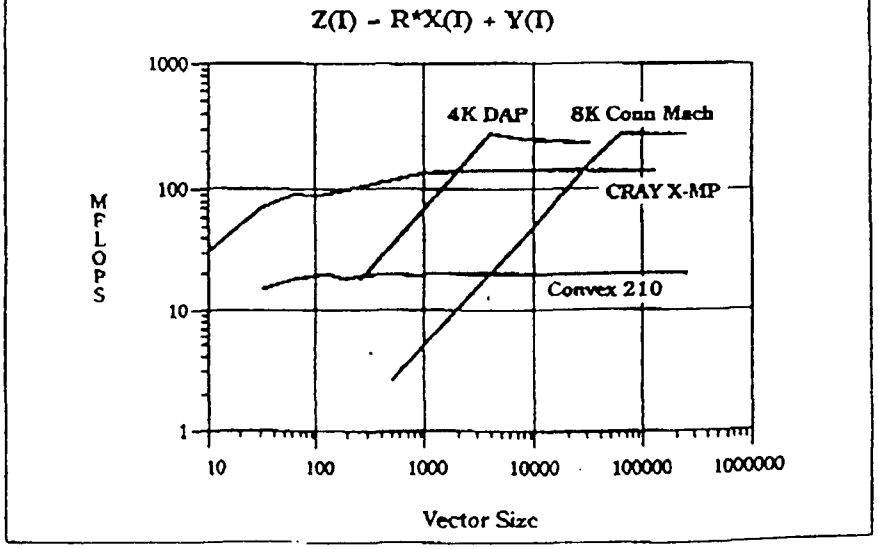
In any case it is only to be expected that quite different architectures would have different computation profiles, i.e., be relatively effective or ineffective on differing sections of the overall computation spectrum, as suggested heuristically in Figure 1 (where 'Computation Spectrum' is intended to suggest a wide range of computation tasks and parameter ranges).

Figure 1: Profiles of Processor Types



In addition, it is our experience that parameters and data lengths can affect the choice of architecture. Figure 2 demonstrates what we call cross-over points; it shows a CRAY X-MP, CONVEX 210, 8K Connection Machine (with co-processor), and 4K DAP on 32-bit SAXPY (using the compiler, not optimized subroutines).

Figure 2: Cross Over Points for SAXPY



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Naval Ocean Systems Center (NOSC)

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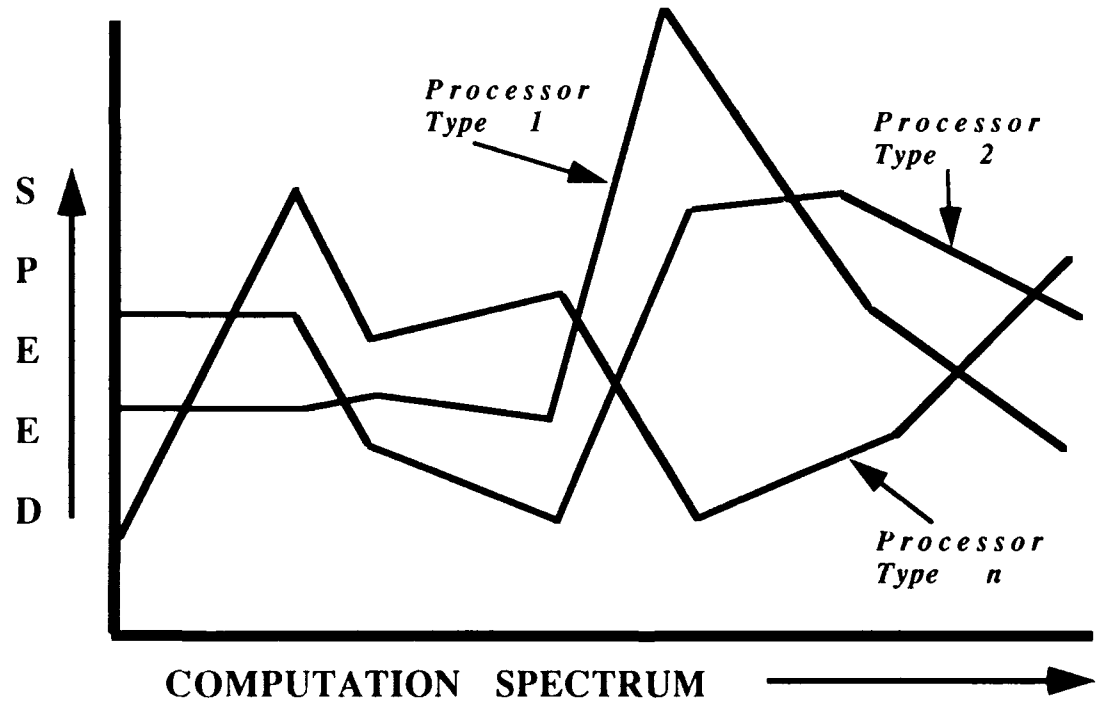

Figure 1. *Profiles of Processor Types*

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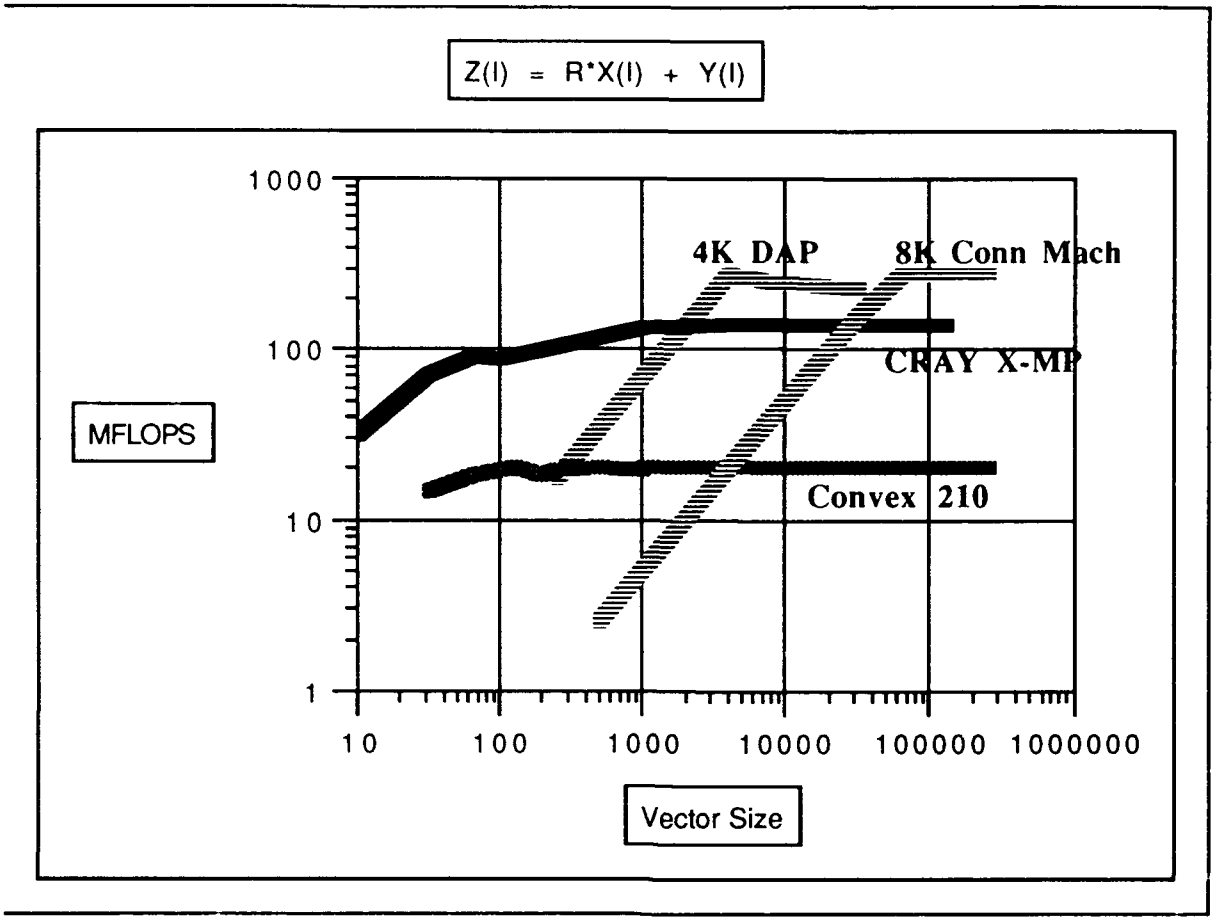

Figure 2. *Cross-over points for SAXPY*

AMDAHL'S LAW The need for DHS arises out of Amdahl's Law, or more precisely, a folk corollary of it:

> *Any single type of super-speed processor used on a heterogeneous code set often spends most of its time on the part it does poorest.*

To illustrate what we mean, suppose we had profiled a large code or set of codes on which we felt distinct, relatively loosely-coupled portions (see "DINS" below) would best be done on quite different architectures, e.g., vector, SIMD, MIMD, special purpose, and data-flow. Let us choose any single processor type, say a CRAY, which is primarily a vector engine. Using the CRAY we might drive the vector portion of the code down to virtually no time, but we would still be left with the non-vector portions (sometimes mistakenly simply called "scalar"). A several-processor CRAY might make modest gains on the MIMD portions and because of its relatively fast scalar processor, it might make some time reductions on the rest of the code. However it would not do nearly as well on these other, non-vector portions as would machines (much less costly than a CRAY) designed for those types of computations. We would be left with the CRAY spending most of its time on the code portions where it achieves only modest improvements. Of course we would obtain similar results if we chose any single processor type which would do well on its kind of code and only fair on other code types. We believe that a more sensible approach is to build a team of processor types that match the computation requirements, as illustrated in Figure 3.

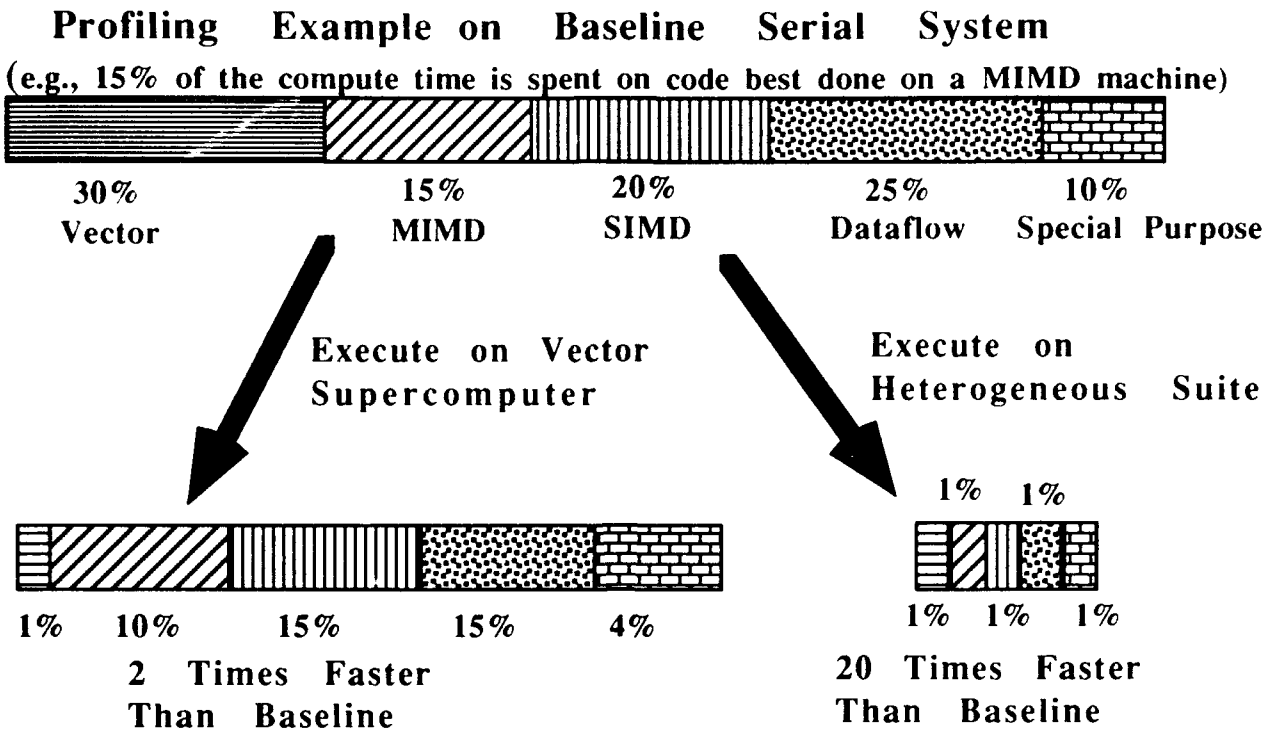

Figure 3. *Code Profiling and Machine Matching*

RESPONSES This effects of Amdahl's Law have been considered before and there are a set of traditional responses.

i. One response is to change the relative percentages of the code types. Suppose we wish to compute with only a vector machine and 35% of the execution time of our code (on some baseline serial system) is naturally vectorizable. Often one can work on changing the algorithm and code to increase this percentage. Typically, however, this approach achieves only modest benefits, say an increase to 50% vectorizable, and often takes a great deal of programmer effort.

ii. Another response has been single processor augmentation, e.g., bringing in a special second computer, such as an array processor, to handle suitable portions of the code. Typically this approach still leaves significant code portions that are not optimal matches to either the main processor or the special purpose machine (and therefore dominant in the overall timings).

iii. Our belief is that a more natural response is to use a tuned suite of heterogeneous processors. Thsi approach attempts to cover all the main types of computation required and to orchestrate effectively the use of the different processors. The potential advantages of this are clear; we optimize the match of all the different portions of code to processor types (wrt compute time) and potentially achieve much higher speeds than the use of any single supercomputer, however powerful.

TRENDS We perceive (Figure 4) four main trends in the development of supercomputing.

i. Device technology -- Advances in basic component technology, primarily density, size, and speed.

ii. Pipelining and vectorization -- Techniques for both scalar and vector hardware to compute at the (asymptotic) rate of one result per clock cycle.

iii. Homogeneous parallelism -- Use of one basic type of parallel design to solve a problem set.

iv. Distributed Heterogeneous Supercomputing -- The combined and orchestrated use of different vector and parallel processors to solve an application set with diverse computation requirements.

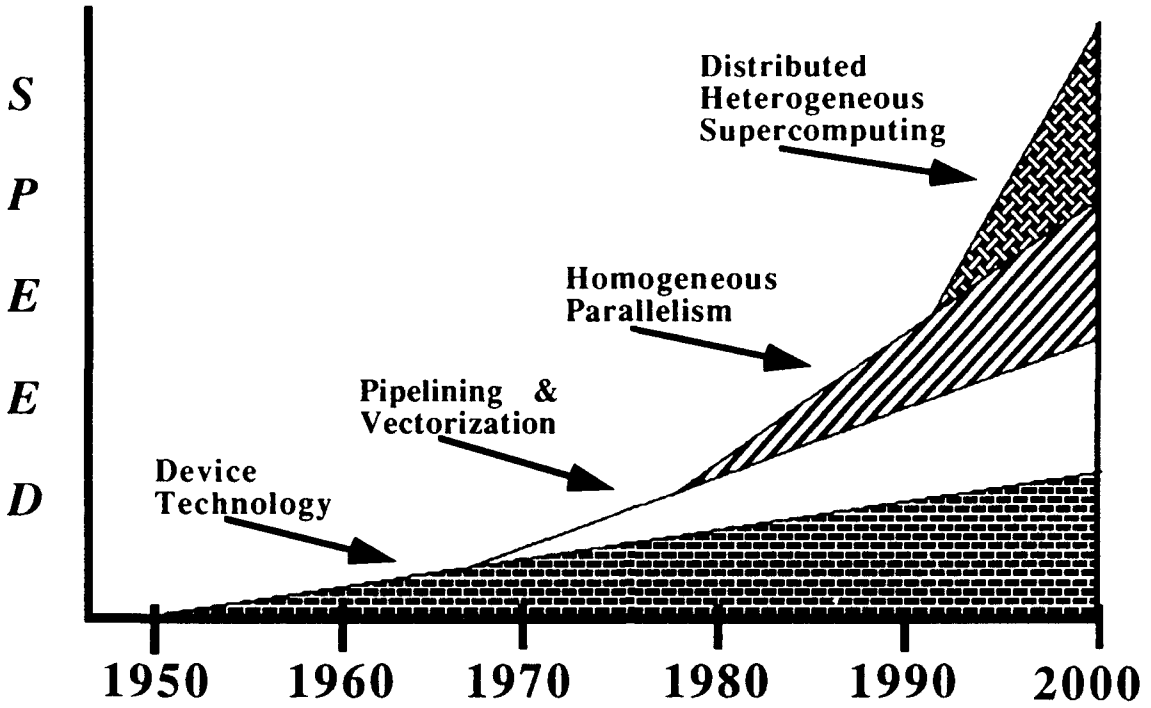

Figure 4. *Supercomputing Trends*

FORMS We see three distinct and potentially complementary forms of Distributed Heterogeneous Supercomputing in the near future.
i. Global DHS -- Heterogeneous processing done over a large geographical area, e.g., the Concurrent Supercomputing Project at JPL/CalTech (Figure 5A). This approach can be used not only to optimize computation speed, but also to maximize the use of remote data bases or display/interface capabilities.
ii. Site DHS -- Mid-sized DHS at one site. This form is currently being implemented at NOSC (Figure 5B).
iii. Micro DHS -- DHS in the small, in which all the diverse processors take the form of different processing functionality in one physical box, e.g., the Purdue mixed-mode PASM [1]. We anticipate seeing new ventures in this arena in the next few months, e.g., an Encore-DAP, with the conscious aim of developing self-contained, tightly-integrated, and tailorable superconcurrent processing (Figure 5C).

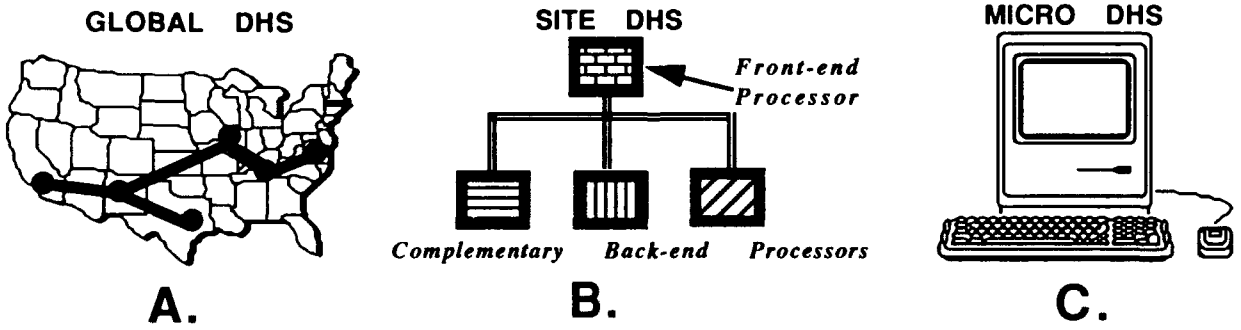

Figure 5. *Forms of DHS*

SUPERCONCURRENCY Superconcurrency is a form of DHS emphasizing performance gains resulting from optimally-configured vector and parallel mini-supers. The Superconcurrency Research Team at NOSC is evaluating this technology for Navy Command and Control problems as described in [2]. Superconcurrency is a general technique for matching and managing optimally configured suites of super-speed processors. In particular the reference demonstrates a general method (actually a mathematical program - eq 1. below) for choosing the most powerful suite of heterogeneous parallel and vector supercomputers for a given problem set, subject to a

fixed constraint, such as cost. The dual problem could find a minimal cost configuration for a fixed speed requirement.

$$\text{MINIMIZE } \mathcal{T} = \sum_{j=1}^{N} \min_{1 \le i \le M} \left(\frac{t_{i,j}}{v_i} \right)$$
$$\text{such that } \sum_{i=1}^{M} v_i \, c_i \le \mathcal{C} \qquad (1)$$

where N = # different code types, M = # different processor types, v_k = total # processors of type k, c_k = cost of processor type k, $t_{l,k}$ = time for processor l on code type k, $\mathcal{T}$ is the total time (function to be minimized), and $\mathcal{C}$ is the overall cost constraint. This approach, called the Optimal Selection Theory is mathematically dependent on new methodologies of code profiling and analytical benchmarking, as suggested by Figures 1 & 3 above.

DINS OR DYNAMIC OPTIMIZATION One of the most active current research areas of the NOSC Superconcurrency Research Team has been the development of the Distributed Intelligent Network System (DINS) concept. DINS will be a reasoning system, built upon an existing distributed O/S, that uses information from Code Profiling, Analytical Benchmarking, and network bandwidth to optimally manage a network of heterogeneous, high-performance, concurrent processors and assigns portions of code to appropriate processors. Superconcurrent implementations will work at the lowest level granularity compatible with the bandwidths available at any given site and the degree of coupling required by the various code modules. Put another way, equation 1 above will actually use $t'_{i,j}$ where the t' reflect not only the actual compute time for processor i on code type j, but the required interprocessor communication time as well:

$$\text{MINIMIZE } \mathcal{T} = \sum_{j=1}^{N} \min_{1 \le i \le M} \left(\frac{t'_{i,j}}{v_i} \right) \qquad (2)$$

In a general sense, this approach is similar to current research in load balancing and priority assignment. However the information sources will be the Profiling, Benchmarking, and bandwidth factors with the primary aim of optimal matching of code portions to processors rather than (the secondary) factors of load balancing and priority assignment. Since DINS will reason about processors actually available to it, we have the potential to achieve configuration control at different sites even though there may be a different superconcurrent suite at each. Similarly DINS will continue to function and assign a second best processor if a first choice is unavailable or down. Thus DINS is robust and survivable. Likewise it is compatible with evolutionary development; when a new processor is introduced because of changing technology, the old benchmarking data can be replaced with the new. The features of robustness, configuration control, survivability, tailorability, and evolutionary development are essential for many Navy problems. We call DINS dynamic optimization since it will dynamically task, in an optimal way, the backend suite of heterogeneous, superconcurrent processors that are chosen by the Optimal Selection Theory.

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REFERENCES

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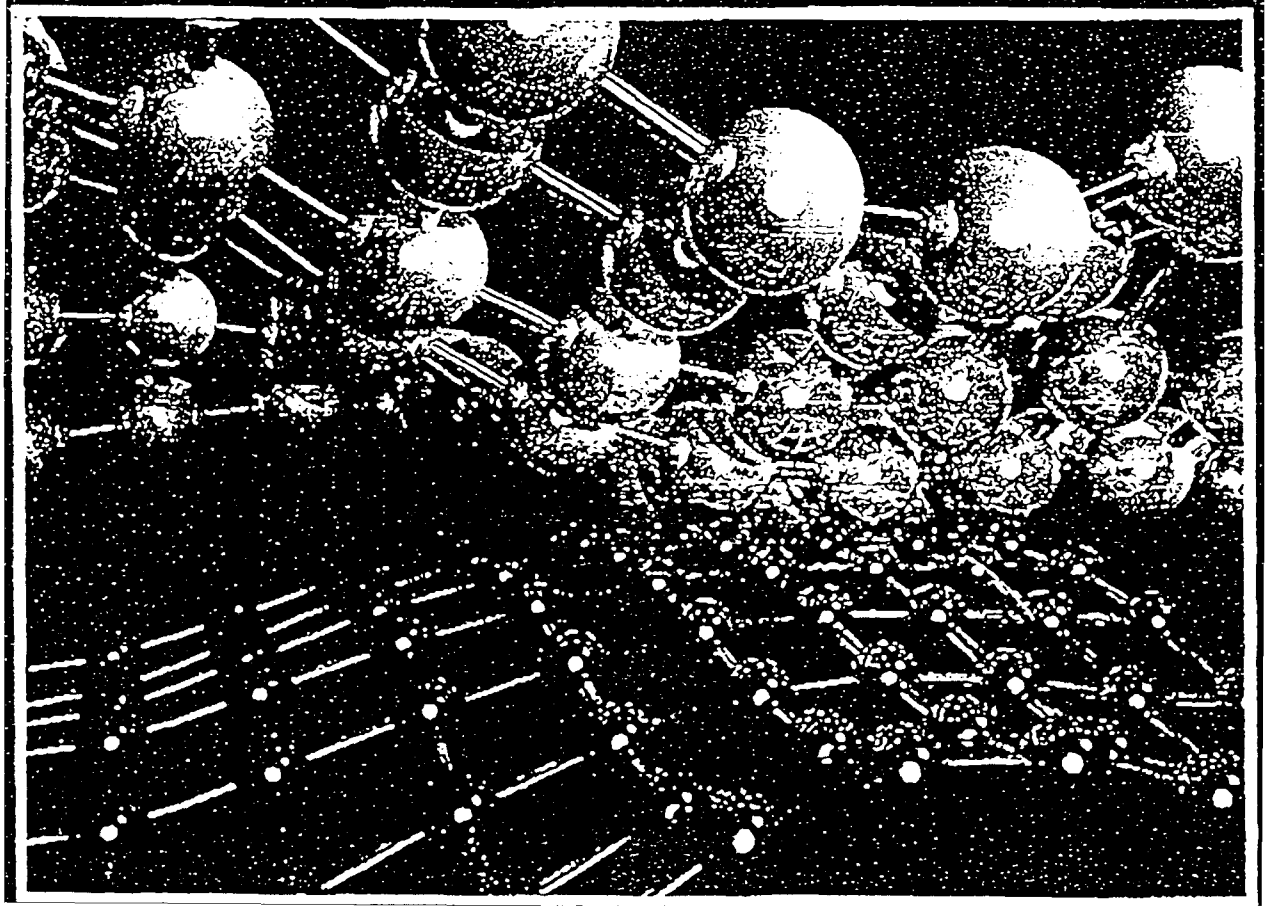

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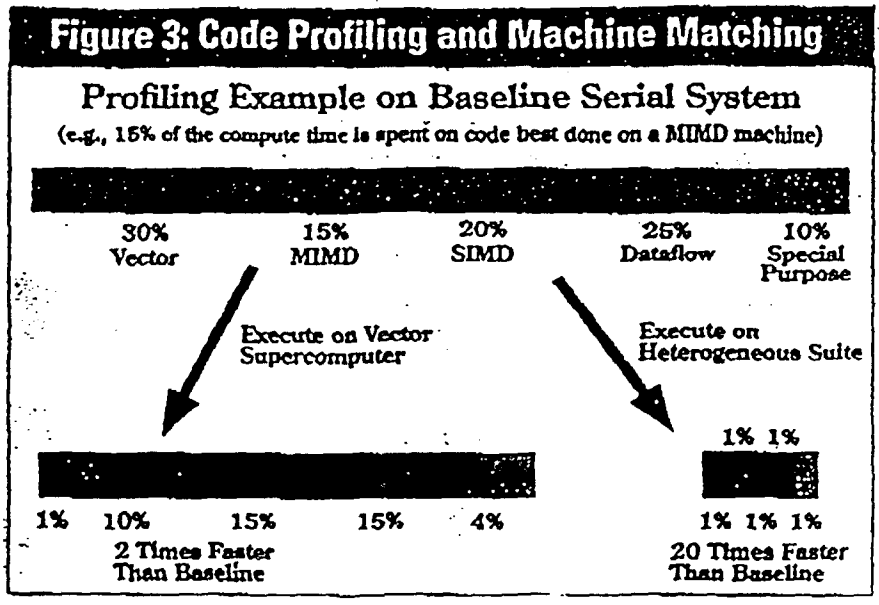

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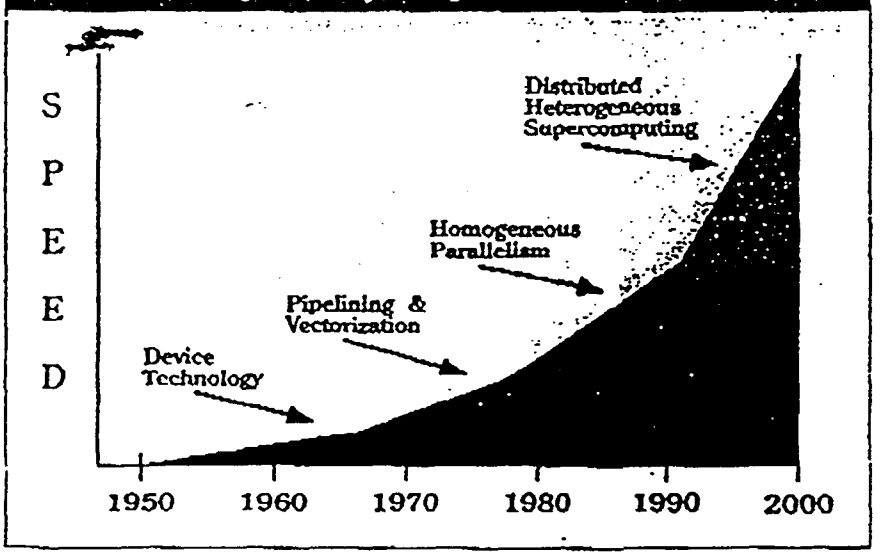

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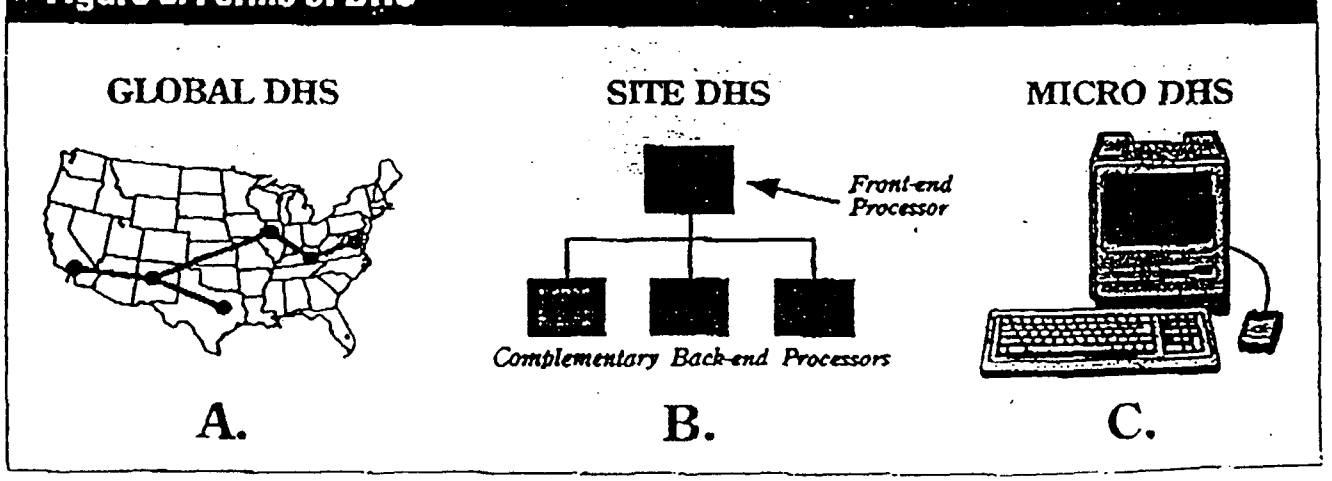

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